

LHCb ECAL/HCAL and Preshower front-end chips PRR

Review report

Orsay, December 12th 2001

Reviewers : Dominique BRETON (ex officio), Jorgen Christiansen, Eric Delagnes, Christophe de la Taille.

Dear colleagues.

You'll find hereafter the reviewers' comments consecutive to the PRR of the Ecal/Hcal and Preshower front-end chips. In general, all of them congratulate the designers both for the quality and the originality of the work performed and for the clearness of the presentations.

General.

Purchasing of quantities close to the final one needed seems quite dangerous to the reviewers. 10% spares could appear too little for safety reasons. Any nasty accident with a crate power supply could destroy a certain amount of chips. Nobody really knows how long the AMS 0.8um BiCOMS technology will stay in production. It's thus suggested to investigate thoroughly the additional cost of making 50% or even 100% more chips than really needed. The additional cost may in fact not be that large. Both kind of chips being encapsulated in a plastic package, it would be necessary to store them in an inert atmosphere after the test in order to let them wait safely for the eventual mounting on the boards.

It was also pointed out that once completed, all the designs will have to be properly stored in the LHCb EDMS database ...

ECAL/HCAL front-end chip.

The reviewers have some worries about possible drifting working levels of the integrator related to the fact that the signal shapes are unipolar. The subtraction of the input signal delayed by 25ns may not be perfectly matched to the original signal because of imperfections in the delay line. Moreover, the fact of having AC coupling between the input buffer and the integrator could also have some effects. This could in the end result in some drifting of the working level of the integrator. This in principle is supposed to be corrected by the digital subtraction of the smallest of the two preceding samples but it must be insured that neither the integrator nor the ADC gets into any kind of saturation. The decay time of the integrator of ~5us will obviously play a significant role in limiting such effects but it would be nice to perform a simulation of the whole chain including the ADC with a very conservative channel occupancy (e.g. 50 %).

The production test limits are based on statistics on a first chip batch. Acceptance limits should normally be set from requirements, not from measurements on a limited set of chips. It would also be advantageous if the production testing were made with test pulses resembling real PMT signals.

It was mentioned that the Icon based integrator resistor could be very sensitive to leakage currents. This should be verified on chips which have had to undergo radiation levels a factor 10 higher than the expected total dose during 10 years of operation. More generally, the irradiated chips should undergo a complete characterization cycle, complemented by a power supply current measurement.

The 100ohm resistor at the ADC input is supposed to avoid the saturation of its input stage. Is this really needed, whereas this has as a consequence to increase the dynamic range required for the chip, and consequently the power supply amplitude ?

A power supply of +4v /-3v is rather wide compared to the dynamic range actually used (1.4 volt). This will obviously result in additional power consumption. Was this voltage difference of 7V really mandatory ? There is indeed another serious implication, the latter being linked to the specifications of the AMS 0.8u (1) technology concerning the chip supplies :

- maximum operating voltage : 5.5V for every junction except the NPN base-emitter one.
- absolute maximum rating : 7V for every junction except the NPN base-emitter one.

In the same specification documents, it's specified that concerning the absolute maximum ratings, "these ratings are stress ratings only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (eg hot carrier degradation, oxide breakdown)."

The conclusion of the reviewers about this point is consequently that if the calorimeter electronics wants to preserve a good reliability, it seems mandatory to enforce the voltage values specified as "the maximum operating voltage". Applying these rules to the chip leads to the statement that they are respected for most of the transistors, excepted :

- the collector to substrate junction of the output NPN
- the bulk of most of the PMOS transistors included in the integrator and in the ICON to the substrate.
- In a much marginal way the collector to substrate junction of the left transistor of the input buffer which is connected to VDD through only 500 ohms (and this only in some of the worst cases)

Most of these problems could easily be solved by the adjunction of serial resistors between VDD and the concerned points. It's to be noticed that in any case, the lack of respect of the specifications may lead to the appearance of leakage currents, the latter being moreover likely to increase with the time. It's also to be noticed that the last versions of the AMS kits give a warning when detecting these violations during the simulation.

It sounds thus necessary to ask AMS about their opinion concerning the potential impact of these violations over the long term reliability of the chips. If the answer is pessimistic, and taking into account the experiment schedule which doesn't seem to be too stringent, the reviewers suggest that a new prototype of this chip including these modifications should be envisaged before launching the production phase.

Two other points were specifically addressed :

Worst cases : the variations in the noise and in the transfer function of the chip depending on the worst cases appear enormous (for instance +50% for the noise : is this linked to a change in the bandwidth or to some ringing ?). There was no real explanation described during the review. The reviewers think it would be interesting to further investigate this phenomena in order to understand it. In particular, they think it would be useful to perform worst case simulations on every individual component of the design to fix the origin of the problem.

Test bench : the reviewers believe it should be useful to measure the chip consumption, especially in the current situation where components are used around or even above their maximal voltage supply levels. They also think it would be fruitful to identify individually all the chips and to store the test measurements results whether the chips are identified as good or bad. In case of any problem encountered later on the front-end boards, this database could become very helpful ...

On the current test bench, there isn't any actual measurement of the signal's plateau. Would it thus be conceivable to inject a shorter test pulse at the chip input ? This pulse shouldn't have to be compulsorily of exponential nature.

Preshower front-end chip.

The preshower front-end chip seems to have been very carefully designed. It is fully differential and includes built in offset compensation circuits. It thus seems to have a performance that largely exceeds the requirements of the Preshower itself.

However, the major worrisome point is its high power dissipation with regard to its placement on a very small and confined board, especially in some worst cases. It's thus kind of a pity not to have foreseen an external adjustment for the bias current, which would have allowed people to decrease the overall power consumption if necessary, even if the correlated drawback would have been a slight decrease in the chip's performance (like the linearity). There is indeed a huge margin in this domain (0.1% compared to the PM's 5% for the non-linearity). The correlated cooling aspects must consequently be carefully investigated. The use of a 800mw IC in a small package is really not evident.

The idea of using as a test bench a board whose design is close to the one of the VFE board is appealing. However, with the testing setup using "DC" signals, it is a bit difficult to determine if the setup really offers sufficient testing capabilities for the production validation. A test setup based on PMT like signals would be more "intuitive". Moreover, a power supply current measurement seems mandatory. This parameter is indeed critical at the system level, and may besides reveal problems affecting the long term reliability of the chip.

As mentioned during the presentations, the integration of the signal charge is very sensitive to the timing of the clock signal relatively to the phase of the input signal. This problem is more related to the detector and the PMT, but it should be verified that the time alignment does not get too critical for use in the final system.

Seen the large power consumption of the chip, the choice of the type of package is a crucial element. The EDQUAD package is a very good candidate. However, it has to be proven that the chip is compatible with this kind of package before launching the production. Similarly, one has to verify that compatible sockets can be found.

Obviously, before launching the production phase, it's mandatory to wait for the results of the irradiation tests. As for the calorimeter chip, it's essential to perform a new complete characterization of the irradiated chips, this including the power consumption.

Sincerely yours.

Dominique.