

# Calorimeter electronics review report

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## Reviewers:

Veljko Radeka, BNL

(John Elias, Fermilab, prevented to come because of cancelled flight)

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## Presentations:

<http://doc.cern.ch/age?a01232>

The reviewers would like to congratulate the LHCb calorimeter group for having prepared an excellent set of presentations for the review. The general architecture of the front-end electronics for the calorimeter system is considered to be sound and well organized. The analog front-end chips seems to have been designed with great care which in most cases have been well confirmed by prototype tests and beam tests. The digital processing of digitized detector signals seems to be well defined and should not pose significant technical difficulties in its implementation.

The question of SEU in the digital logic has been taken into account by partitioning the digital implementation into discrete memories with error correction, when justified, and FPGA's with minimum sensitivity to upsets (anti-fuse based). The interface to the L0 calorimeter trigger system seems well defined and well adapted to the implementation of the front-end electronics.

## General:

All front-end chips for the four sub-detectors are based on the same technology (AMS 0.8 um BiCMOS). This has the advantage that experience from the different chips can easily be exchanged between designers. It though makes the whole calorimeter system very vulnerable to the potential disappearance of this technology. The Calorimeter group must monitor closely the status of this technology. Being a technology with more than 5 years of age there is a significant risk that it may disappear rather quickly. Production of chips should be made as early as possible and sufficient quantities of spares must be acquired. The ECAL/HCAL and the Preshower chip seem to be nearly ready for production. The SPD front-end chip still seems to require a significant development time (1 - 2 years). The development of the SPD front-end chip can possibly be shortened if an external cable driver is used.

The status of the AMS technology must be closely monitored and in case of possible obsolescence alternative technologies (more modern) must be found.

The ECAL/HCAL chip production is foreseen in Sept-Oct 2001 and the PS chip in the first half of 2002. It is indeed foreseen to use an external cable driver and multiplexer for the SPD chip. We therefore think production can be done early enough (2002?)

The calorimeter electronics uses extensively the programmable delay chip from the CERN MIC group. It must be insured that an agreement with the MIC group is made to insure delivery of these special IC's.

Contact was established with Marchioro. A few chips can be loaned for SEU tests which however cannot take place before Sept-Oct 2001. A new production can be launched after. This chip however doesn't comply with the LHCb official requirements for readback possibility this can be especially delicate if tests demonstrate strong SEU sensitivity. In this case another solution will be studied.

A policy on spare parts of specialized components must be defined to insure maintenance over a time period of ~10 years.

OK we'll do it within the coming year.

An analysis of how the calorimeter detectors plan to perform synchronization to the beam crossings would be useful. Binary detectors (SPD) can be especially problematic in this respect.

The SPD is not especially difficult compared with the other detectors. But it is true that we should simulate how with LED calibration system and beam this will be done for all detectors. A note will be produced within the coming year. A group has been formed to define the diode system(s?)

It must be insured that all setup registers and LUT's have read back to be capable of doing basic system tests. It was not clear if the front-end chip for the SPD is planned to have read back of all its setup registers.

The channel threshold registers will be readable.

Nothing was mentioned about power supplies for the electronics in the cavern. Special care must be taken to insure that the required power supplies can work reliably in the radiation environment in the cavern or the required power can be delivered with sufficient quality from distant power sources (counting room). This may be especially difficult for the high power crates containing the 9U front-end modules. It must be insured that an appropriate strategy for power distribution (place for wires, global/local regulation, location of power supplies) and cooling is determined before the construction of the detector and its electronics begins.

Correct: studies have started and contact with companies. It is important to find out if a place "shielded from neutron irradiation" (for example below the calorimeters) can be found at < 40 meters from the crates. We need calculations on the neutron flux.

It was not presented how the gain stability of the PM's and the front-end electronics can be monitored (supposedly a part of detector calibration which was not discussed in detail during the review).

A calibration note exist (supporting note for the TDR LHCb 2000-051) Once the LED system is better understood the note will be updated (mid 2002?)

Large gain variations (factor 4) between PM's (or channels in same PM) are assumed to be corrected by adjustable resistors on the base plate of the PM's. It will require quite some manual work to perform this adaptation and it should be considered if a programmable approach could not be implemented at an acceptable cost.

This is only the case for the PS/SPD 200 64-anode PM which have to be measured anyhow. We think a more complicated DAC system is unrealistic. It will increase the power consumption and the area in SPD and PS design.

It should be remembered that the SPD threshold and PS calibration are adjustable. A relative change in gain not recoverable by HV adjustment "only" results in loss of dynamic range until the PM+base+load system is replaced.

SEU problems seem to have been taken well into account in the design of the electronics. Total dose effects and potential single event latch-up problems must be evaluated with proper radiation tests of prototype implementations.

Fully agreed ! In general the collaboration agrees on the need of more calculations on neutron flux and plans to carry them out as soon as the manpower becomes available.

It must be insured that all final designs are properly documented and transferred to an EDMS archive. (EDMS archiving of LHCb electronics is in fact not yet well defined).

We agree . A tutorial on EDMS is planned this year in LHCb.

## Trigger:

It must be insured that it is possible to mask the contribution of dead/noisy channels to the calorimeter trigger (either in front-end or in calorimeter trigger system).

Dead channels will not trigger, and there is nothing to mask. Their effect should be taken care of by Monte-Carlo.

Noisy channels if ECAL and HCAL can be easily masked by filling the LUT (converting ADC to 8 bit transverse energy) with zeroes.

Masking PreShower and SPD should be implemented at a similar location on the Preshower front-end board, i.e. when preparing the trigger data.

It must be insured that all data used by the calorimeter trigger system, to make a trigger decision, is also read out so the functions of the trigger system can be confirmed off-line ( for verification of trigger system and calculation of trigger efficiencies). Special care must be taken for this when data is zero-suppressed or different encoding schemes are used for readout and for the trigger (e.g. compression to floating point).

We are considering a direct reading by the DAQ of the trigger input data for ECAL and HCAL cards. If this is too expensive, one should make the zero suppression smarter, to not lose information, and probably send the raw information on those channels having a non-zero contribution to the trigger. Note that the good functionality of the trigger is checked during special tests, with programmed inputs and logging of the partial outputs in FIFO which are read-back by ECS. For Preshower and SPD the bits will be readout independently of the zero suppression.

A large number of links between front-end boards are used to implement the required first stage of trigger processing on the front-end cards. It might be worth studying the possibility of using serial links for all data transfers on the back-plane, also for the neighbors. It could be an advantage having only one type of transmission mechanism, provided that the additional effort and board space for the components is not prohibitive.

There is no reason to use those chips where data transfer is obvious. Optimization studies have already been performed as proven during the review.

The high connectivity between boards via the back-plane and LVDS links pose a challenge to get a reliably working system. It is emphasized that testing of these connections are made as early and thoroughly as possible.

Thorough simulations have already been performed. The backplane itself is under design and a prototype will be also thoroughly tested before mid 2002.

## Ecal/Hcal:

The final front-end cards (especially 32 channel E/Hcal cards) with the required trigger pre-processing seems to be very dense and complicated modules. Special testing methods for high complexity boards using surface mount and BGA packages must be incorporated in the designs (e.g. JTAG boundary scan).

We'll try to totally avoid the use of BGA packages. Thus the boundary scan doesn't seem to be that helpful for card debug. We rather believe testability goes through well chosen access to data all along the data paths.

## Pre-shower and scintillating pad detector (SPD):

The cooling requirements of the SPD and pre-shower very front-end must be analyzed in more detail and potential cooling schemes must be worked out.

There should be manpower available to do this study in the last quarter of 2001.

## Critical components to be reviewed separately when appropriate:

Front-end chip for E/Hcal, before production (Production readiness review).

Front-end chip for preshower, before "final" prototype/production (Production readiness review).

Front-end chip for SPD, before "final" prototype/ production (design review and Production readiness review).

Final E/Hcal front-end board, before starting production. (Production readiness review).

Final Preshower/SPD front-end board, before starting production. (Production readiness review).

Power distribution and cooling.

No problem in principle but the number style and form of reviews should be decided.  
If we do 6 reviews of electronics per LHCb subdetector, we will rapidly run out of reviewers!